APPLIED PHYSICS LETTERS VOLUME 72, NUMBER 10 9 MARCH 1998

Modulation doping of InAs/AlSb quantum wells using remote InAs donor layers

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(Received 16 October 1997; accepted for publication 8 January 1998)

Sheet carrier concentrations in quantum wells of InAs clad by AlSb were enhanced by modulation doping with very thin (9–12 Å) remote InAs(Si) donor layers. The growth temperature of the donor layers was a key parameter, with relatively low temperatures required to minimize Si segregation into the AlSb. Sheet carrier concentrations as high as $3.2\times10^{12}/\mathrm{cm}^2$ and $5.6\times10^{12}/\mathrm{cm}^2$ were achieved by single- and double-sided modulation doping, respectively. High electron mobility transistors fabricated using the modulation doped structure exhibited a unity current gain cut-off frequency of 60 GHz for a 0.5 μm gate length at a source-drain voltage of 0.5 V.
[S0003-6951(98)01010-9]

Single quantum wells of InAs clad by AlSb are of interest for application to high-speed, low-voltage, high electron mobility transistors (HEMTs). Advantages of this material system include the high electron mobility ($30\,000\ \mathrm{cm}^2/\mathrm{V\,s}$) and velocity ($4\times10^7$ cm/s) of InAs,[1] and a large conduction band offset between InAs and AlSb (1.35 eV). Promising HEMT characteristics have been reported, with a unity current gain cut-off frequency, f_T, of 90–100 GHz for 0.5 μm gate lengths.[2,3]

Sheet carrier concentrations for unintentionally doped InAs/AlSb single quantum wells, a function of the upper barrier thickness and cap material (InAs or GaSb), are typically in the range $0.4-1.6\times10^{12}/\mathrm{cm}^2$.[4] Densities can be increased to $1.5-2.2\times10^{12}/\mathrm{cm}^2$ by an As-soak technique.[5,6] Higher sheet charge densities are desirable for HEMT applications. Si is the most common *n*-type dopant in III-V molecular beam epitaxy (MBE) systems. Si is, however, amphoteric in the III-V's, producing *n*-type GaAs, InAs, AlAs, and InSb, but *p*-type GaSb and AlSb.[7] Chalcogens such as Te have been used as an *n*-type dopant in AlSb, resulting in sheet carrier concentrations as high as $3.8\times10^{12}/\mathrm{cm}^2$ in InAs/AlSb HEMTs.[8] A disadvantage of introducing Te into a MBE system is its high vapor pressure and the resulting memory effects.

An alternative to chalcogen doping of GaSb and AlSb is Si doping of a remote, thin InAs quantum well. Malik *et al.*[9] applied this technique to InAs/GaSb quantum wells and achieved densities as high as $3.6\times10^{12}/\mathrm{cm}^2$. Kudo and Mishima[10] formed InAs/$\mathrm{In_{0.5}Al_{0.5}As_{0.56}Sb_{0.44}}$ quantum wells and modulation doped the $\mathrm{In_{0.5}Al_{0.5}As_{0.56}Sb_{0.44}}$ with Si. They obtained sheet densities of $1.2\times10^{12}/\mathrm{cm}^2$ but the room-temperature mobility was only $4600\ \mathrm{cm}^2/\mathrm{V\,s}$. Bolognesi *et al.*[11] used InAs/AlSb superlattices as barriers for an InAs quantum well and doped selected InAs layers with Si to obtain a sheet carrier density of $1.3\times10^{12}/\mathrm{cm}^2$ and a room-temperature mobility of $30\,000\ \mathrm{cm}^2/\mathrm{V\,s}$. Recent work by Sasa *et al.*[12] achieved sheet carrier concentrations in the $2-4\times10^{12}/\mathrm{cm}^2$ range by Si planar doping in a 6 monolayer (ML) InAs quantum well located 80 Å below a 150 Å InAs quantum well clad by AlGaSb.

In order to achieve high carrier concentrations in InAs/AlSb quantum wells, we designed a structure in which a very thin (2–7 ML) layer of Si-doped InAs is inserted 125 Å above a 150 Å InAs well (Fig. 1). The large confinement energy of the thin quantum well allows the electrons to transfer into the 50 ML InAs channel. By lowering the growth temperature to minimize Si segregation, we achieved carrier densities up to $3.2\times10^{12}/\mathrm{cm}^2$. HEMTs fabricated using this material displayed good dc and microwave characteristics. In addition, structures with InAs(Si) donor layers on both sides of the InAs quantum well yielded sheet carrier concentrations as high as $5.6\times10^{12}/\mathrm{cm}^2$.

Samples were grown by solid-source MBE using $\mathrm{As_2}$ from a valved As cracker. Both a conventional $\mathrm{Sb_4}$ cell as well as an Sb cracker producing $\mathrm{Sb_2/Sb_1}$ were used. Growth temperatures were measured by transmission thermometry.[13] The GaAs and AlSb buffer layers were grown at 580 °C and 530 °C, respectively, at a rate of 1.0 ML/s. The undoped InAs and adjacent AlSb were grown at a rate of 0.5 ML/s and a temperature near 500 °C. The growth temperature of the InAs(Si) donor layer and 15 Å AlSb immediately above it was varied from 360 to 500 °C. The As valve was closed during all AlSb layers to minimize As incorporation. Migration-enhanced epitaxy was used at interfaces between InAs and AlSb to achieve InSb-like bonds.[5,14]

Transport measurements were made at 300 K and 77 K using a conventional 5×5 mm Van der Pauw structure and a field of 2100 G. Selected samples were also patterned into

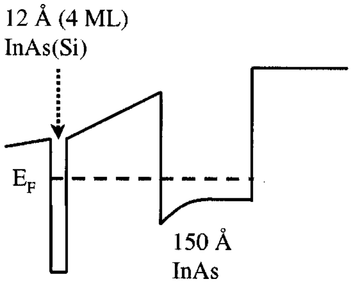

FIG. 1. Schematic of band structure for modulation InAs(Si) doping of InAs/AlSb quantum wells.

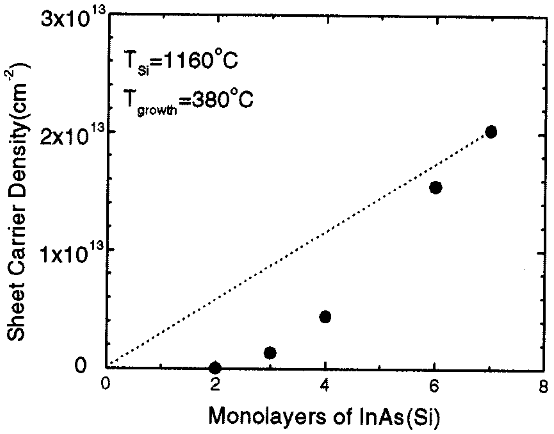

FIG. 2. Sheet carrier density as a function of donor layer thickness for InAs(Si) layers clad by AlSb. The 2 ML sample was highly resistive. The dotted line indicates the expected carrier density based upon the 7 ML value and the assumption of negligible Si segregation.

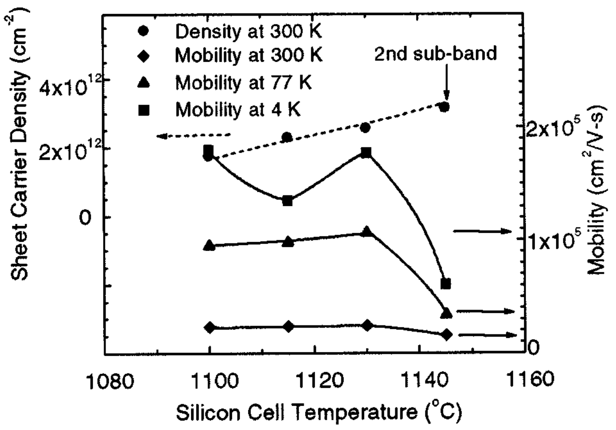

FIG. 3. Sheet carrier density and mobility as a function of silicon cell temperature for 50 ML InAs/AlSb quantum wells remotely doped by 4 ML InAs(Si) layers. The InAs(Si) layers were grown at 380 °C. Lines are guides to the eye.

standard Hall bridges with 100 μm channel widths using photolithography. Quantum Hall measurements were carried out at 4.2 K.

First, we investigated structures with the thin InAs(Si) well but without the 150 Å undoped well. The complete heterostructure (from cap-to-substrate) was: 20 Å InAs/100 Å AlSb/6–21 Å InAs(Si)/2 μm AlSb/0.5 μm GaAs/GaAs(SI)-(001). The first set of four samples was grown with 4 ML InAs(Si) layers and a Si cell temperature of 1130 °C.[15] For InAs(Si) growth temperatures of 450 and 500 °C, the samples were highly resistive ($>10^6\ \Omega$/sq). For temperatures of 365 and 420 °C, however, the transport measurements yielded sheet carrier densities of 0.9×10^{12}/cm^2 and 1.0×10^{12}/cm^2, respectively. (As expected for thin layers, the mobilities were very low, with $\mu_{300}\sim100$ cm^2/V s.) These results suggest that Si from the InAs layer is segregating into the AlSb during growth at the higher growth temperatures. Because Si is predominantly an acceptor in AlSb, Si atoms segregating into the AlSb will compensate Si donors remaining in the InAs. If over 50% of the Si segregates into the AlSb as acceptors, we would expect a highly resistive sample, as observed at the higher growth temperatures. Segregation is an activated process; hence, the dependence on growth temperature is reasonable.

To further investigate the role of Si segregation, we grew a second set of samples with the substrate temperature fixed at 380 °C and a Si cell temperature of 1160 °C. The thickness of the InAs(Si) layer was varied. In Fig. 2, we plot the room-temperature sheet carrier density as a function of InAs(Si) thickness. Samples with 2, 3, 4, and 6 ML InAs(Si) are included. An additional sample consists of 7 ML InAs(Si) with an undoped ML of InAs on either side. The density increases with increasing InAs(Si) thickness but is not linear. The density for 7 ML is 2.02×10^{13}/cm^2. If only a small amount of segregation is occurring in this sample (a reasonable approximation given the densities of the 6 ML and 7 ML samples), we would expect 1.15×10^{13}/cm^2 for the 4 ML layer, compared to the measured value of 0.44×10^{13}/cm^2. These results are consistent with substantial Si segregation from the InAs(Si) monolayers adjacent to the AlSb. Apparently, over half of the Si segregated into the AlSb for the 2 ML sample, resulting in a resistive layer. For the 6 ML InAs(Si) sample, assuming no Si segregation, we obtain a carrier density of 8.6×10^{19}/cm^3. Densities as high as 5×10^{19}/cm^3 were reported for thick layers of Si-doped InAs.[16]

Based upon the above results, we selected a growth temperature of 380 °C and a thickness of 4 ML for the InAs(Si) donor layers. A set of four samples was grown with the InAs(Si) donor layers and undoped InAs wells; the Si flux was varied. The complete heterostructure (from cap-to substrate) is:

> 20 Å InAs(cap)/100 Å AlSb/12 Å InAs(Si)/125 Å AlSb/150 Å InAs/2 μm AlSb/0.5 μm GaAs/GaAs(SI)-(001).

Results are shown in Fig. 3 where we plot sheet carrier concentration at 300 K and mobility at 300 K, 77 K, and 4 K versus Si cell temperature. For the first three samples, carrier concentrations range from 1.7 to 2.6×10^{12}/cm^2 with room-temperature mobilities of 23 000–25 000 cm^2/V s. The fourth sample has a sheet carrier concentration of 3.2×10^{12}/cm^2 and a mobility of 16 000 cm^2/V s.[17] Quantum Hall measurements show no evidence of a parallel conduction channel in the Si-doped InAs layers for these four samples. Only a single sub-band is occupied for the first three samples. A second sub-band is occupied for the most heavily doped sample, apparently causing the reduction in mobility. At 4 K, the carrier densities in the two sub-bands are 2.56×10^{12}/cm^2 and 0.17×10^{12}/cm^2.

We estimated the carrier density required to occupy the second sub-band. The first two sub-band energies for a 150 Å InAs well are calculated to be 60 meV and 182 meV at 0 K when the nonparabolicity, strain, and penetration effects are taken into account.[18] Integrating the density-of-states yields 1.75×10^{12}/cm^2, in reasonable agreement with our experimental value of 2.39×10^{12}/cm^2 and the Sasa *et al.*[12] value of 2.0×10^{12}/cm^2.

We also investigated structures with 4 ML InAs(Si) layers on both sides of an undoped InAs quantum well. The doped layers were grown at 380–400 °C and separated from the InAs by 125 Å AlSb. Otherwise, the structures were identical to those described previously. For a Si cell temperature of 1100 °C, the room-temperature density and mobility

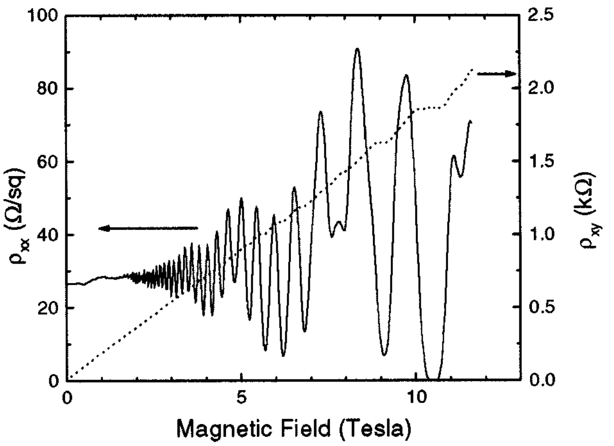

FIG. 4. Shubnikov–de Haas oscillations for a sample with InAs(Si) donor layers on both sides of an undoped InAs quantum well. Two sub-bands are occupied, with sheet carrier densities of $3.01\times 10^{12}/\mathrm{cm}^2$ and $0.54\times 10^{12}/\mathrm{cm}^2$ at 4 *K*.

are $4.05\times 10^{12}/\mathrm{cm}^2$ and 16 200 $\mathrm{cm}^2/\mathrm{V\,s}$, respectively. Low-temperature quantum Hall effect measurements are shown in Fig. 4. Two components are observed in the Shubnikov–de Haas oscillations, yielding carrier densities in the two sub-bands of $3.01\times 10^{12}/\mathrm{cm}^2$ and $0.54\times 10^{12}/\mathrm{cm}^2$ and a mobility of 65 500 $\mathrm{cm}^2/\mathrm{V\,s}$. A second sample was grown with an identical structure and higher Si flux (cell temperature of 1140 °C). The room-temperature density and mobility are $5.60\times 10^{12}/\mathrm{cm}^2$ and 13 400 $\mathrm{cm}^2/\mathrm{V\,s}$, respectively, yielding a sheet resistance of 83 Ω/sq.

A heterostructure with a single InAs(Si) layer above the undoped InAs was grown and processed into a HEMT. The donor layer consisted of 2 ML InAs(Si) followed by a single ML of undoped InAs. The room-temperature sheet density and mobility were $2.5\times 10^{12}/\mathrm{cm}^2$ and 17 100 $\mathrm{cm}^2/\mathrm{V\,s}$, respectively. Using this material, HEMTs with a gate length, L_g, of 0.5 μm were fabricated with *e*-beam lithography. Additional fabrication details for similar HEMTs are given elsewhere.[3]

A typical set of drain characteristics for the HEMTs is shown in Fig. 5. For this device, the gate width is 28 μm and the source-drain spacing is 1.2 μm. A high drain current density is observed which results from the combination of high sheet charge density in the channel and low access resistance. The low-field source-drain resistance at $V_{GS}=0$ V is 0.46 Ω mm. The devices also display good pinchoff at $V_{GS}=-1.6$ V and negligible kink effect. The lack of saturation in the drain current is believed to be primarily due to the accumulation of holes generated by impact ionization in the channel which serves to reduce carrier depletion. A maximum transconductance of 1.6 S/mm is measured at $V_{DS}=1$ V. Using *S*-parameter measurements, an f_T of 60 GHz is obtained at $V_{DS}=0.5$ and $V_{GS}=-1.1$ V, corresponding to an extrinsic $f_T L_g$ product of 30 GHz μm. At this bias condition, the gate leakage current was 140 μA. Reduction of this relatively high leakage and improved current saturation should be achievable through advancements in the material design as has been previously reported.[3]

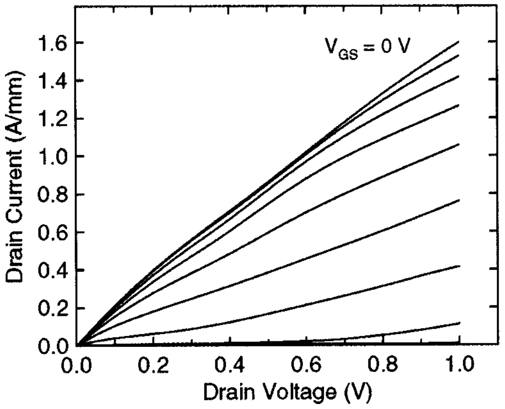

FIG. 5. HEMT drain characteristics for a device with a sheet carrier density of $2.5\times 10^{12}/\mathrm{cm}^2$; $L_g=0.5\ \mu$m, $L_{SD}=1.2\ \mu$m, $W_G=28\ \mu$m, $V_{GS}=0.2$ V/step.

Note added in proof: Recently, Zhao *et al.* reported AlSb/InAs HEMTs with planar Si doping in a 30 Å InAs layer beneath the channel.[19]

The authors thank W. Kruppa and R. J. Wagner for technical discussions. This work is supported by the Office of Naval Research.

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